**Web**

Results 1 - 2 of about 3 for **(multiple channels) "(glitch free reset signal)"**. (0.31 seconds)

Tip: Try removing quotes from your search to get more results.

[PDF] HardCopy Device Handbook, Volume 1

File Format: PDF/Adobe Acrobat

... The HardCopy Stratix devices use the same base arrays across **multiple** designs for a given density and are customized using the top two metal layers. ...

www.hcyy-ic.com/data/hb/hc_h5v1.pdf - Supplemental Result - [Similar pages](#)

[PDF] HardCopy Series Handbook, Volume 1

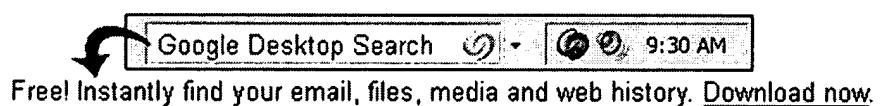
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... 15-13 Replacing One or More FPGAs With One or More HardCopy Series Devices in a **Multiple**- Device Configuration Chain ...

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If you like, you can [repeat the search with the omitted results included](#).

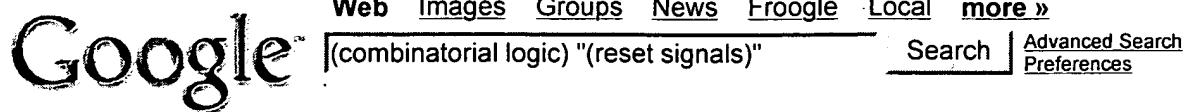


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**Web**Results 1 - 100 of about 592 for **(combinatorial logic) "(reset signals)"**. (0.47 seconds)

Tip: Save time by hitting the return key instead of clicking on "search"

[PPT] SMEX*lite COMPUTATION HUB ARCHITECTURAL REVIEWFile Format: Microsoft Powerpoint 97 - [View as HTML](#)Signals generated in **combinatorial logic** paths are never used to clock storage... **Reset signals** should be removed synchronously to ensure that all clocked ...klabs.org/richcontent/MAPLDCon00/Presentations/Session_P/P1_Albajes_S.ppt - [Similar pages](#)**[PDF] Lessons Learned from FPGA Developments**File Format: PDF/Adobe Acrobat - [View as HTML](#)synchronous part contained other signals than the usual clock and **reset signals**.This kind of ... propagate to cause output error in **combinatorial logic** ...klabs.org/DEI/lessons_learned/esa_lessons/esa_fpga_001_01-0-0.pdf - [Similar pages](#)**[PDF] FPGAs in Critical Applications and Model Support**File Format: PDF/Adobe Acrobat - [View as HTML](#)Gate level mitigation - **logic**. **combinatorial logic**. sequential. **logic** ...next state record. current state record. clock signals. **reset signals** ...www.estec.esa.nl/wsmwww/mpd2004/FTMR-xilinx.pdf - [Similar pages](#)**Patent 4221927: Voice responsive "talking" toy****combinatorial logic** means responsive to said pseudo-random code signal, ...The various clock and **reset signals** of particular frequency referred to herein ...www.freepatentsonline.com/4221927.html - [Similar pages](#)**Patent 5321827: Computer system with modular upgrade capability**The signal is generated by **combinatorial logic** in FIG. 3 illustrated as **logic**elements ... 8), in turn generated from **reset signals** from the system board. ...www.freepatentsonline.com/5321827.html - [Similar pages](#)[More results from www.freepatentsonline.com]**Enter CLB Logic Power Information**To enter CLB (Configurable Logic Block) **Logic** Power Information: ... Data-path**logic** uses **combinatorial logic** (multiplexers, adders, AND gates, ...www.xilinx.com/ise/power_tools/wpt_help/app_docs/enter_clb_logic_power_information.htm - 10k -[Cached](#) - [Similar pages](#)**[PDF] Xilinx DS063: XC9500 In-System Programmable CPLD Family Data Sheet**File Format: PDF/Adobe Acrobat - [View as HTML](#)global clock, output enable, and set/reset signals. The FB. generates 18 outputs that drive ... **Combinatorial Logic**. Internal System Cycle Time = T. SYSTEM ...www.xilinx.com/bvdocs/publications/DS063.pdf - [Similar pages](#)[More results from www.xilinx.com]**EP617513 At european software patent - Field programmable gate ...**For example, typical **logic** functions include **combinatorial logic**, adders, ...

Local and global set/reset signals are provided via an OR gate 506 to the ...

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